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09/461,643	12/14/1999	KEITH DOW	10559/108001	4089

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2189	17

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPL

Office Action Summary	Application No.	Applicant(s)	
	09/461,643	DOW, KEITH	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10-14,16-20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-14,16-20,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *15 April 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 15th of April, 2003. Claims 1, 8, 14 and 20 have been amended; claims 21 and 22 have been canceled; and claims 23 and 24 have been newly added. Currently, claims 1, 3-8, 10-14, 16-20, 23 and 24 are pending in this application.

Claim Objections

2. Claim 14 is objected to because of the following informalities: In the claim, the limitation "forming at least two parallel layers on a surface of a circuit board, with first and second signal lines on a first layer of the board" doesn't make sense to one of ordinary skill in the art of PCB technologies because the multiple layers for routing signals, which is disclosed by the Applicant, cannot be implemented on a surface (i.e., the exterior or upper boundary of an object or body) of a circuit board. Instead, the multiple layers could be implemented in parallel to the surface of the circuit board. Therefore, the limitation would be considered as --forming at least two parallel layers to a surface of a circuit board, with first and second signal lines on a first layer of the board-- by the Examiner for the purpose of the claim rejection based on a prior art. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 20 recites the limitation "the distance separating the lines" in lines 18-19 (Amendment filed on 15th of April, 2003, page 8, lines 13-14). There is insufficient antecedent basis for the subject matter "the distance" of the limitation in the claim. Therefore, the limitation could be considered as --a distance separating the lines-- by the Examiner for the purpose of the claim rejection based on a prior art.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 4-8, 11-14, 16-20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Perino et al. [US 6,160,716 A; hereinafter Perino].

Referring to claim 1, AAPA discloses a computer system 100 (Fig. 1) comprising: processor (i.e., CPU 105 of Fig. 1); a memory unit (i.e., memory hub 110 of Fig. 1) configuring to store data used by said processor (See Fig. 1 and page 1, lines 10-13; i.e., wherein in fact that the computer including CPU, memory unit, MCU, and MCU controlling the flow of data into and out of memory unit implies said memory unit configuring to store data used by said processor); a memory control unit (i.e., memory control unit 120 of Fig. 1) configured to manage data flowing into and out of said memory unit (See page 1, lines 12-13), a circuit board (See Fig. 1 and Fig. 2; i.e., in fact, all the components within said computer systems are fabricated on a circuit board, which is well known to one of ordinary skill in the art of personal computer system at the time the invention was made. Especially, AAPA teaches a part of circuit board routing geometry between said MCU and said memory unit, as shown in Fig. 2) comprising: a first signal line (i.e., signal line 150 of Fig. 2), formed on a first layer of said circuit board (e.g., surface layer on said circuit board) and connected between a first pin (i.e., pin 155 of Fig. 2) on said memory unit and said memory control unit (See page 2, lines 3-8); and a second signal line (i.e., signal line 160 of Fig. 2) also formed on said first layer (e.g., said surface layer on said circuit board) of said circuit board and connected to said first pin on said memory unit (See page 2, lines 8-10), a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2; Note the definition of the term "acute" in dictionary states -ending in a sharp point: as being or forming an angle measuring less than 90 degrees-,

Merriam Webster's Colligiate Dictionary by Merriam-Webster, Inc.") relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not teach said circuit board comprising a second portion of said second signal line substantially parallel to a second portion of said first signal line; at least two layers formed in parallel to a surface of said circuit board, and wherein said first layer defines a non-grounded gap between said first and second signal lines.

Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1) comprising a portion of a signal line (i.e., trace 870 of Fig. 8, Example B) substantially parallel to a portion of another signal line (i.e., trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B); at least two layers (e.g., signal traces' plane and a ground plane) formed in parallel to a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of said circuit board (See col. 4, lines 62-67), and wherein a layer (i.e., surface layer of motherboard 110 of Fig. 1) defines a non-grounded gap between first and second signal lines (See Fig. 8, Example B, Fig. 16, and col. 4, lines 66-67 and col. 7, lines 21-26; i.e., wherein in fact that a ground plane is on the backside of the motherboard, and those figures implies that a ground gap is not between said first and second signal lines).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32), and (2)

eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 4, Perino teaches said first signal line and the portion of said second signal line that is routed substantially parallel to said first signal line (i.e., the portion of trace 870 and the portion of trace 880 are in parallel in Fig. 8, Example B; Perino) have substantially equal widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 5, Perino teaches said first signal line and the portion of said second signal line that is routed substantially parallel to said first signal line (i.e., the portion of trace 870 and the portion of trace 880 are in parallel in Fig. 8, Example B; Perino) are separated by a distance (i.e., 8 mils space in Fig. 8, Example B) substantially equal to said widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 6, AAPA, as modified by Perio, discloses all the limitations of the claim 6 including said width of said lines are each substantially equal to 5 mils (See AAPA, page 2, lines 7-9) except that does not teach said distance separating said lines are each substantially equal to 5 mils. However, the claim 6 recites the subject matter "said distance separating said lines are each substantially equal to 5 mils" without any patentable advantage in the specification (See the claim 6 and amended specification (filed on 14th of August, 2002) page 2, lines 8-20), such as the reason of 'substantially equal to 5 mils rather than 8 mils' with any patentable advantage. Therefore, the subject matter 'substantially equal to 5 mils' in the claim is not patentably significant since it at most relates to the width of space between said signal lines under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Referring to claim 7, AAPA disclose said memory unit is a Rambus device (See page 1, line 19 through page 2, line 2).

Referring to claim 8, the method steps of claim 8 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 8.

Referring to claim 11, the method steps of claim 11 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 11.

Referring to claim 12, the method steps of claim 12 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 12.

Referring to claim 13, the method steps of claim 13 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 13.

Referring to claims 14 and 16, the method steps of claims 14 and 16, are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claims 14 and 16.

Referring to claim 17, the method steps of claim 17 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 17.

Referring to claim 18, the method steps of claim 18 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 18.

Referring to claim 19, the method steps of claim 19 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 19.

Referring to claim 20, AAPA discloses a circuit board (See Fig. 1 and Fig. 2; i.e., in fact, all the components within said computer systems are fabricated on a circuit board, which is well known to one of ordinary skill in the art of personal computer system at the time the invention was made. Especially, AAPA teaches a part of circuit board routing geometry between said MCU and said memory unit, as shown in Fig. 2) for use in a computer system (Fig. 1) comprising: a memory unit (i.e., memory hub 110 of Fig. 1); a memory control unit (i.e., memory control unit 120 of Fig. 1); and a data bus connecting said memory control unit to said memory unit (i.e., bus between memory control unit 120 and memory hub 110 in Fig. 1) and comprising: a first signal line (i.e., signal line 150 of Fig. 2) formed on a first layer of said circuit board (e.g., surface layer on said circuit board) and connected to said memory control unit and to a first pin on said memory unit (See page 2, lines 3-8; i.e., connection between a pin 155 of Fig. 2 on

memory unit 110 of Fig. 1 and memory control unit 120 of Fig. 1); and a second signal line (i.e., signal line 160 of Fig. 2) formed on said first layer (e.g., said surface layer on said circuit board) of said circuit board and also connected to said first pin connection on said memory unit (See page 2, lines 8-10), a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2) relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not teach said circuit board comprising a second portion of said second signal line substantially parallel to a second portion of said first signal line; at least two layers formed in parallel to a surface of said circuit board, wherein said width of said lines and a distance separating said lines are each substantially equal, and wherein said first layer defines a non-grounded gap between said first and second signal lines.

Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1) comprising a portion of a signal line (i.e., trace 870 of Fig. 8, Example B) substantially parallel to a portion of another signal line (i.e., trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B); at least two layers (e.g., signal traces' plane and a ground plane) formed in parallel to a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of said circuit board (See col. 4, lines 62-67), wherein said width (i.e., 8 mils signal line in Fig. 8, Example B) of said lines (i.e., the portion of trace 870 and the portion of trace 880 in Fig. 8, Example B; Perino) and a distance (i.e., 8 mils space in Fig. 8, Example B) separating said lines are each substantially equal (i.e., 8 mils in Fig. 8, Example B), and wherein a layer (i.e., surface layer of motherboard 110 of Fig. 1) defines a non-grounded gap between first and second signal lines (See Fig. 8, Example B, Fig. 16, and col. 4, lines 66-67 and col. 7, lines 21-26; i.e., wherein in fact that a ground plane is on the backside of the motherboard, and those figures implies that a ground gap is not between said first and second signal lines).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32), and (2) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 23, AAPA teaches said memory unit comprises a memory repeater hub (See page 1, line 12; i.e., memory hub 110 of Fig. 1).

Referring to claim 24, AAPA teaches said memory unit comprises a memory repeater hub (See page 1, line 12; i.e., memory hub 110 of Fig. 1).

7. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino [US 6,160,716 A] as applied to claims 1, 4-8, 11-14, 16-20, 23 and 24 above, and further in view of Theus [US 4,904,968].

Referring to claim 3, AAPA, as modified by Perino, discloses all the limitations of the claim 3 except that does not teach third and fourth signal lines, on a second layer of said circuit board, different than said first layer.

Theus discloses a circuit board configuration for reducing signal distortion, wherein third and fourth signal lines (e.g., signal traces 26 and 32 in Fig. 4), on a second layer (e.g., signal layer 30 of Fig. 4) of said circuit board, different than a first layer (e.g., signal layer 20 of Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said multiple layered circuit board, as disclosed by Theus, for said circuit board, as

disclosed by AAPA, as modified by Perio, for the advantage of providing an improved circuit board for reducing signal distortion characteristics (See Theus, col. 4, lines 6-8).

Referring to claim 10, the method steps of claim 10 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 10.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 3-8, 10-14, 16-20, 23 and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Erbele [US 5,012,390] discloses mounting and connection system for electrical communications equipment.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL
May 22, 2003

MARK H. RINEHART
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